

[SYSTEM ON CHIP]

Abstract of Disclosure

A system on chip (SOC) characterized by nitride read only memory (NROM) and read only memory (ROM) has a P-type substrate, and at least an NROM area and a read only memory area defined on the surface of the substrate. ONO layers are disposed along a first direction and positioned in the NROM area and the read only memory area. A bit line is positioned in the substrate between each ONO layer. Oxide layers are positioned atop each bit line. A plurality of word lines disposed along a second direction covers each ONO layer in the NROM area and the read only memory area, so as to form a plurality of NROM cells at the intersection of the NROM area and each ONO layer, and to form a plurality of read only memory cells at the intersection of the read only memory area and each ONO layer. A doping area is optionally positioned at a bottom side of a read only memory cell, so as to cause the read only memory cell to have at least two different threshold voltages and to form ROM code.

Figures

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100